What is claimed is:

1. An integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug, comprising:

a substrate;

a spare cell, disposed in the substrate, the spare cell comprising at least one input terminal and at least one output terminal;

a plurality of metal layers, disposed over a surface of the substrate;

a top-layer output terminal pad, disposed in a top metal layer of the plurality of metal layersand electrically coupled to the output terminal of the spare cell by a via structure; and

a top-layer input terminal pad, disposed in the top metal layer and electrically coupled to the input terminal of the spare cell by the via structure.

2. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 1, wherein the spare cell has a preset logic function, adapted for ECO and FIB debug.

3. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 1, wherein when the FIB debug is performed, the top-layer input terminal pad and the top-layer output terminal are coupled to an output terminal of a previous-stage circuit and an input terminal of a next-stage circuit respectively for enabling the spare cell.

4. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 1, wherein when the ECO is performed, the top-layer input terminal pad and the top-layer output terminal are coupled to a top-metal layer previous-stage circuit and a top-metal layer next-stage circuit respectively for enabling the spare cell.

5. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 1, wherein at least one inter-medium metal layer is disposed between the top metal layer and the substrate; the via structure further comprises an inter-medium metal terminal pad on the inter-medium metal layer; the inter-medium metal terminal pads of the via structure coupled to the output terminal and the input terminal are an inter-medium output terminal pad and an inter-medium input terminal pad, respectively; and when the ECO is performed, the inter-medium input terminal and the inter-medium output terminal are coupled to an inter-medium metal previous-stage circuit and an inter-medium metal next-stage circuit for enabling the spare cell.

6. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 1, wherein the top-layer input terminal pad is coupled to a ground voltage by the via structure.

7. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 1, wherein the top-layer input terminal pad is coupled to a system power voltage by the via structure.

8. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 7, wherein when the FIB debug is performed, an ion beam is used to cut an electrical connection between the top-layer input terminal pad and the system power voltage; and the top-layer input terminal pad and the top-layer output terminal pad are coupled to an output terminal of a previous-stage circuit and an input terminal of a next-stage circuit respectively for enabling the spare cell.

9. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 7, wherein when the ECO is performed, a top system power voltage terminal pad is removed to cut an electrical connection between the top-layer input terminal pad and the system power voltage; and the top-layer input terminal pad and the top-layer output terminal are coupled to a top-metal layer previous-stage circuit and a top-metal layer next-stage circuit respectively for enabling the spare cell.

10. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 7, wherein at least one inter-medium metal layer is disposed between the top metal layer and the substrate; the via structure further comprises an inter-medium metal terminal pad on the inter-medium metal layer; the inter-medium metal terminal pads of the via structure coupled to the output terminal, the input terminal and the system power voltage are an inter-medium output terminal pad, an inter-medium input terminal pad and an inter-medium system power voltage terminal pad, respectively; when the ECO is performed, the inter-medium system power voltage terminal pad is removed to cut an electrical connection between the top-layer input

terminal pad and the system power voltage; and the inter-medium input terminal and the inter-medium output terminal are coupled to an inter-medium metal previous-stage circuit and an inter-medium metal next-stage circuit for enabling the spare cell.

11. The integrated circuit adapted for Engineering Change Order (ECO) and Fiber Ion Beam (FIB) debug of claim 7, wherein the integrated circuit is a Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuit.